CLAIMS

What is claimed is:

1. An apparatus for performing digital-to-analog conversion, comprising:

first and second current steering digital-to-analog converters (DAC), each DAC having a first and second output forming a differential DAC output; and

switch circuitry, wherein the switch circuitry couples the differential output of at most a selected one of the first and second DACs to a pair of switch nodes, wherein the differential output of a non-selected one of the first and second DACs is shorted.

2. The apparatus of claim 1 wherein the switch circuitry comprises:

a first switch coupled to selectively short the differential output of the first DAC in response to a first clock signal; and

a second switch coupled to selectively short the differential output of the second DAC in response to a second clock signal.

3. The apparatus of claim 2 wherein the first and second clock signals collectively form a non-overlapping multiphase clock signal, wherein only one of the first and second switches is open at any time.

4. The apparatus of claim 2 wherein the first and second clock signals form a non-overlapping multiphase clock signal to ensure that at any time at least one of the first and second DAC differential outputs is shorted.

5. The apparatus of claim 2 wherein the first and second DACs and the switch circuitry reside on a same semiconductor substrate.

6. The apparatus of claim 1 further comprising:

a differential amplifier having a differential input communicatively coupled to the pair of switch nodes.

7. The apparatus of claim 6 further comprising:

buffer circuitry coupled to the first and second switch nodes and the differential amplifier, wherein the buffer circuitry isolates the differential input of the differential amplifier from direct connection to the pair of switch nodes.

8. The apparatus of claim 1 wherein a second output of the first DAC and the first output of the second DAC are connected at a first common node, wherein the first and second switches share a second common node.

9. The apparatus of claim 8 further comprising:

level shifting circuitry coupling the first and second common nodes.

10. The apparatus of claim 8 wherein a sum of the first and second outputs of each DAC is a substantially constant value I_{DC}, wherein the first common node is connected to a current source of a same constant value I_{DC}.

11. A subscriber line analog front end circuit apparatus, comprising:

first and second current steering digital-to-analog converters (DAC), each DAC having a first and second output forming a differential DAC output;

switch circuitry, wherein the switch circuitry couples the differential output of at most a selected one of the first and second DACs to a pair of switch nodes, wherein the differential output of a non-selected one of the first and second DACs is shorted; and

a differential amplifier having a differential input communicatively coupled to the pair of switch nodes, the differential amplifier having a differential output coupled to drive a tip line and a ring line of a subscriber line.

12. The apparatus of claim 11 wherein the subscriber line is a digital subscriber line.

13. The apparatus of claim 11 wherein the switch circuitry comprises:

a first switch coupled to selectively short the differential output of the first DAC in response to a first clock signal; and

a second switch coupled to selectively short the differential output of the second DAC in response to a second clock signal.

14. The apparatus of claim 13 wherein the first and second clock signals collectively form a non-overlapping multiphase clock signal, wherein only one of the first and second switches is open at any time.

15. The apparatus of claim 13 wherein the first and second clock signals form a non-overlapping multiphase clock signal to ensure that at any time at least one of the first and second DAC differential outputs is shorted.

16. The apparatus of claim 11 wherein the first and second DACs, the switch circuitry, and the differential amplifier reside on a same semiconductor substrate.

17. The apparatus of claim 11 further comprising:

buffer circuitry coupled to the first and second switch nodes and the differential amplifier, wherein the buffer circuitry isolates the differential input of the differential amplifier from direct connection to the pair of switch nodes.

18. The apparatus of claim 17 wherein the first and second DACs, the switch circuitry, the buffer circuitry, and the differential amplifier reside on a same semiconductor substrate.

19. The apparatus of claim 17 further comprising:

a power amplifier having a differential power amplifier input coupled to a differential output of the differential amplifier; and

interface circuitry coupling a differential output of the power amplifier to the tip and ring lines of the subscriber line.

20. The apparatus of claim 19 wherein the first and second DACs, the switch circuitry, the buffer circuitry, the differential amplifier, and the power amplifier reside on a same semiconductor substrate within a same integrated circuit package, wherein the interface circuitry does not reside within the same integrated circuit package.